# APPENDIX

The "marked-up" version of the amended claims is as follows:

29. (Twice Amended) A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising the steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode, a drain electrode and a data line connected to the source electrode on the semiconductor pattern, wherein the gate insulating layer, the semiconductor pattern and the data wire are patterned in a single photolithography step [so that a portion of the semiconductor pattern between the source electrode and the drain electrode are exposed];

forming color filters made of photosensitive material, the color filters covering data wire[, directly contacting the exposed portion of the semiconductor pattern,] and having a first contact hole; and

forming a pixel electrode connected to the drain electrode through the first contact hole of the color filters.

36. (Amended) The method of claim 35, wherein the gate wire and the data wire are patterned through a photolithography process including only exposure and development steps.

64. (Amended) A thin film transistor array panel for a liquid crystal display, comprising:

a plurality of gate lines formed on an insulating substrate;

a gate insulating layer covering the gate lines;

a plurality of data lines intersecting the gate lines;

an amorphous silicon layer formed under the entire data lines;

an ohmic contact layer interposed between the data lines and the amorphous silicon layer;

an array of thin film transistors, each transistor including a gate electrode connected to the gate line, a source electrode connected to the data line, and a drain electrode;

a plurality of color filters formed over the gate insulating layer, the color filters overlapping the data lines at last in part; and

a plurality of pixel electrodes formed on the color filters, each pixel electrode electrically connected to the drain electrode.

71. (Amended) A thin film transistor array panel for liquid crystal display, comprising:

a plurality of gate lines formed on an insulating substrate;

a first insulating layer covering the gate lines;

a plurality of data lines intersecting the gate lines[, each data line including];

an amorphous silicon layer[,] formed under the entire data lines;

an ohmic contact layer [and a metal layer] interposed between the data lines and the amorphous silicon layer;

an array of thin film transistors, each transistor including a gate electrode connected to

the gate line, a source electrode connected to the data line, and a drain electrode;

a second insulating layer formed at least on the data lines, the second insulating layer contacting a portion of the amorphous silicon layer exposed between the source electrode and the drain electrode; and

a plurality of pixel electrodes formed on the second insulating layer, each pixel electrode electrically connected to the drain electrode.

Please add new claims 75-80, as follows.

75. (New) The thin film transistor array panel of claim 71, wherein said second insulating layer has a contact hole exposing a portion of one of the data lines near an end of the one of the data lines.

76. (New) The thin film transistor array panel of claim 75, further comprising a redundant data pad contacting the exposed portion of the data lines through the contact hole.

77. (New) The thin film transistor array panel of claim 75, wherein the redundant data pad is made of the same layer as the pixel electrodes.

78. (New) The thin film transistor array panel of claim 71, wherein said first insulating layer and said second insulating layer has a contact hole exposing a portion of one of the gate lines near an end of the one of the gate lines.

79. (New) The thin film transistor array panel of claim 78, further comprising a redundant gate pad contacting the exposed portion of the gate lines through the contact hole.

80. (New) The thin film transistor array panel of claim 79, wherein the redundant gate pad is made of the same layer as the pixel electrodes.

80. (New) The thin film transistor array panel of claim 79, wherein the redundant gate pad is made of the same layer as the pixel electrodes.

## REMARKS

In response to the Office Action dated June 19, 2002, claim 66 has been cancelled, claims 36, 64 and 71 have been amended, and claims 75-80 have been newly added. Claims 1-12, 29-49 and 64-65 and 67-80 are active in this application, of which claims 1, 29, 34, 37, 38, 46, 64 and 71 are independent. The Office Action indicates that claims 1-12, 34 and 38-45 are allowed, and claims 31-33, 47-49 and 69-70 are allowable but objected to for being dependent from the rejected base claims.

Entry of the Amendments and Remarks is respectfully requested because entry of Amendment places the present application in condition for allowance, or in the alternative, better form for appeal. No new matters are believed to be added by this Amendments. Based on the above Amendments and the following Remarks, Applicants respectfully request that the Examiner reconsider the outstanding objections and rejections and they be withdrawn.

### *Rejections Under 35 U.S.C. §112*

In the Office Action, claims 36, 37, 68 and 74 have been rejected under 35 U.S.C. §112, second paragraph. This rejection is respectfully traversed.

Regarding claims 36 and 37, the Examiner states that the claim language is incomplete because the expression "through only exposure" omits what the material is exposed to. It is submitted that the terms "exposure" and "development" are commonly used in the photolithography technology, and thus specifying the material to which the gate wire and the

data wire are exposed during the photolithography process would unnecessarily limit the claim scope to an exposure process involving a certain material.

To clarify that the exposure and development are used in the extent of a photolithography process, in this response, claim 36 has been amended to recite "the gate wire and the data wire are patterned through a photolithography process including only exposure and development steps". Thus, Applicants respectfully request that the rejection under 35 U.S.C. §112, second paragraph over claims 36 and 37 be withdrawn.

Regarding claims 68 and 74, the Examiner states that these claims omit essential structural cooperative relationships of elements because the relative position of said conductive pattern overlapping said storage electrode. Particularly, the Examiner asserts that it is not clear how both layers could be formed of the same layer and overlap each other at the same time.

Independent claim 64 recites "a plurality of gate lines formed on an insulating substrate; a gate insulating layer covering the gate line; a plurality of data lines intersecting the gate lines". Dependent claim 67 recites "a storage electrode made of the same layer as the gate line", and dependent claim 68 recites "a conductor pattern overlapping the storage electrode, the conductor pattern made of the same layer as the data lines".

Thus, the storage electrode and the gate lines are made of the same layer, and the conductor pattern and the date lines are made of the same layer. Thus, the conductor pattern may overlap the storage electrode.

Also, it should be noted that claims 64, 66 and 67 do not recite that the conductor pattern and the storage electrode are formed of the same layer, as understood by the Examiner. Claim 74 recites basically the same structure.

Accordingly, Applicants respectfully request that the rejection under 35 U.S.C. §112, second paragraph over claims 68 and 74 be withdrawn.

***Rejections Under 35 U.S.C. §103***

In the Office Action, claims 46, 71 and 72 have been rejected under 35 U.S.C. §103(a) for being unpatentable over U. S. Patent No. 6,022,753 issued to Park, *et al.* ("Park"). This rejection is respectfully traversed.

Regarding claim 46, the Examiner admitted that the photodefinable conductive material as the material type of the gate and data elements is not found in Park. Regarding this missing feature, the Examiner takes a position that Park clearly discloses metallic wires consistent with the definition of the term for one skilled in the art to conclude the similarity of the structures based on material type and method of fabrication. This assertion is respectfully traversed.

As dictated in MPEP 608.01(o), a term used in the claims may be given a *special meaning* in the description although no term may give a meaning repugnant to the usual meaning of the term. In this regard, the term "photodefinable conductive material" (originally "photosensitive conductive material") was used to describe a material with which "an etching step using the photoresist pattern as an etch mask may be omitted, and the gate wires 22, 24, 26 and 28 may be formed by a photolithography process that includes only exposure and development steps" (Specification, Page 20, Lines 12-15) in attempt to simplify the manufacturing process. Thus, in the specification, in the present application, the term "photodefinable conductive material" is given a meaning that is distinguished from conductive materials that required an etch mask during a photolithography process. Thus, Applicants

respectfully request that the term "photodefinable conductive material" be given the meaning in the description pursuant to MPEP 608.01(o).

In this regard, Park fails to explicitly teach or implicitly suggest that the gate wire 200 or data line 600 can be made of a material with which an etching step using the photoresist pattern as an etch mask may be omitted to simplify the manufacturing process. No secondary reference has been introduced to cure this deficiency from the teachings of Park.

For these reasons, it is respectfully submitted that it would not have been obvious to modify the teachings of Park to arrive at the claimed invention. Accordingly, Applicants respectfully request that the rejection over claim 46 be withdrawn.

Regarding claims 71 and 72, independent claim 71 has been amended and now recites "[A] thin film transistor array panel for liquid crystal display, comprising: ... a plurality of data lines intersecting the gate lines; an amorphous silicon layer formed *under the entire data lines*; an ohmic contact layer interposed between the data lines and the amorphous silicon layer; ...".

For example, such feature is shown in Fig. 15, in which "the data wire parts 62, 64, 65, 66, and 68, the ohmic contact layer pattern 55, 56, and 58, and the semiconductor patterns 42 and 48 through one photolithography process" (Specification, Page 17, Lines 16-18).

In this regard, according to Park, the amorphous silicon layer 510 and the amorphous silicon layer 400 are selectively formed only in the source and drain regions, and Park fails to teach or suggest that the data line 600 has an amorphous silicon layer formed *under the entire data lines*; as recited in claim 71.

This is also evidenced by the fact that the storage electrode 640 which is made of the same layer with source and drain electrodes 60 has a single-layer structure, as shown in Fig. 2. Also, Park is silent as to forming the data wire, the ohmic contact layer, and the semiconductor

layer through one photolithography process. No secondary reference has been introduced to cure this deficiency from the teachings of Park, and it would not have been obvious to modify the teachings of Park to arrive at the claimed invention.

Thus, Applicants respectfully submit that claim 71 is patentable over Park, and claim 72 that is dependent from claim 71 would be also patentable at least for the same reason. Accordingly, Applicants respectfully request that the rejection over claims 71 and 72 be withdrawn.

In the Office Action, claims 29, 30, 35-37, 64-68 and 73-74 have been rejected under 35 U.S.C. §103(a) for being unpatentable over Park in view of U. S. Patent No. 6,104,462 issued to Kurosaki, *et al.* ("Kurosaki"). This rejection is respectfully traversed.

Regarding independent claim 29, this claim has been amended to recite "A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising the steps of: .... forming a gate insulating layer ...; forming a semiconductor pattern ...; forming a date wire ..., *wherein the gate insulating layer, the semiconductor pattern and the data wire are patterned in a single photolithography step*".

In this regard, neither Park nor Kurosaki teaches or suggests the claimed feature of patterning the gate insulating layer, the semiconductor pattern and the data wire by a single photolithography step. Therefore, it would not have been obvious to combine the teachings of the applied references to arrive at the claimed invention.

Thus, Applicant respectfully submits that claim 29 is patentable over Park and Kurosaki. Claims 30, 35 and 36 which are dependent from claim 29 would be also patentable at least for

the same reason. Accordingly, Applicants respectfully requests that the rejection over claims 29, 30, 35 and 36 be withdrawn.

Regarding claim 37, this claim has been amended to present in independent form and specifically recite "the gate wire or the data wire is made of *photosensitive conductive material*, and the gate wire and the data wire are patterned through only exposure and development, and are made of *Ag paste or copper organic metal* that includes photoresist".

As previously mentioned, Park fails to teach or suggest the photosensitive conductive material to simplify the processing steps. This missing feature is not cured by the secondary reference to Kurosaki. Particularly, none of the applied references teaches or suggests the particular materials (*Ag paste or copper organic metal* that includes photoresist) recited therein.

For these reasons, it would not have been obvious to combine the teachings of the applied references to arrive at the claimed invention. Thus, Applicants respectfully submit that claim 37 is patentable over Park and Kurosaki, and request that the rejection over claim 37 be withdrawn.

With respect to independent claim 64, in this response, this claim has been amended to further recite "a plurality of data lines intersecting the gate lines; an amorphous silicon layer formed *under the entire data lines*; an ohmic contact layer interposed between the data lines and the amorphous silicon layer; ...". As previously mentioned, Park fails to teach or suggest this claimed feature. This missing feature is not cured by the secondary reference to Kurosaki. Thus, none of the applied references teaches or suggests the data line having a multi-layer structure.

For these reasons, it would not have been obvious to combine the teachings of the applied references to arrive at the claimed invention. Thus, Applicants respectfully submit that claim 64 is patentable over Park and Kurosaki. Claims 65, 67, 68, 73 and 74 that are dependent from claim 64 would be also patentable at least for the same reason.

Accordingly, the Examiner is respectfully requested to withdraw all the outstanding rejections and objections over claims 1-12, 29-49 and 64-65 and 67-80 be withdrawn, and pass those claims to allowance.

## CONCLUSION

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete response has been made to the outstanding Office Action and, as such, claims 1-12, 29-49 and 64-65 and 67-80 are in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

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